IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Recker et al.	Atty. Dkt.: SC11244ZC
Serial No.: 09/654,253	Group Art Unit: 2128
Filed: September 1, 2000	Examiner: DAY, Herng Der
Title: MISMATCH MODELING TOOL	

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: April 1, 2005

DECLARATION UNDER 37 C.F.R §1.131

Sir:

In compliance with 37 C.F.R. §1.131, the following Declaration and any attachments are provided to establish conception in the United States of the Invention (claimed subject matter) in the above referenced patent application (hereinafter "the Subject Application") and due diligence to the filing of the Subject Application on September 1, 2000 from a date prior to August 24, 2000, the effective date of U.S. Patent No. 6,560,755 (hereinafter "the '775 Patent"). In accordance with MPEP 715.07 (C) this Declaration and any attachments is intended as a statement of facts sufficient to show conception of the invention prior to August 24, 2000, the effective date of the '775 Patent, coupled with due diligence from prior to the effective date of the '775 Patent to September 1, 2000, the filing date of the Subject Application (constructive reduction to practice). The '775 Patent was cited by the Examiner in an Office Action dated November 17, 2004 to support a rejection under 35 U.S.C. 103(a) of the claims for the Subject Application.

We, Cynthia L. Recker and Patrick G. Drennan, the undersigned, do hereby depose and sayeth:

1. That we are the named inventors for the claimed subject matter of the Subject Application, that we were at the time of the invention employed by the Semiconductor Products Sector of Motorola, Inc., the original Assignee of the Subject Application, and that we are presently employed by Freescale Semiconductor, Inc., a separate entity created by divestiture that includes the previous Semiconductor Products Sector of Motorola, Inc., and is the present Assignee of the Subject Application.

2. That prior to August 24, 2000, the effective date of the '775 Patent, during the course of employment by the Semiconductor Products Sector of Motorola, Inc., we had conceived of and conceptualized the MISMATCH MODELING TOOL as disclosed and claimed in the Subject Application.

3. That the claimed subject matter of the Subject Application was the subject of a written Patent Disclosure (attached as Appendix I) prepared after conception, and that before August 24, 2000, the effective date of the '775 Patent, the Patent Disclosure was submitted and presented (Presentation attached as Appendix II) to a Patent Committee of Semiconductor Products Sector of Motorola Inc. for consideration and assignment to a patent attorney for preparation and filing of a patent application.

4. That the claimed subject matter of the Subject Application was the subject of one or more draft US Patent Applications (one draft US Patent Application attached with Weiss and Moy cover letter dated August 22, 2000 as Appendix III) and that before August 24, 2000, the effective date of the '775 Patent, the draft US Patent Application was provided to us for our review.

SC11244ZC Declaration under 37 C.F.R. §1.131

5. That on information and belief the Subject Application was finalized and filed, in due course and with due diligence from a date before August 24, 2000, the effective date of the '775 Patent, in the United Stated Patent Office on September 1, 2000 by or on behalf of Semiconductor Products Sector of Motorola Inc.

6. That the Patent Disclosure, Presentation, Weiss and Moy cover letter, and draft US Patent Application are known to us to be true copies which, based on information and belief, evidences such conception and that each of the dates redacted from the Patent Disclosure and Presentation, is prior to August 24, 2000, the effective date of the '775 Patent.

7. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the Subject Application or any patent which issues thereon.

Dated: 4/1/05

Cynthia L. Recker,
Member of the Technical Staff
Freescale Semiconductor, Inc.

Dated: 4/1/05

Patrick G. Drennan
Member of the Technical Staff
Freescale Semiconductor, Inc.

Attachments:

Appendix I

Appendix II

Appendix III

APPENDIX I 1.131 DECLARATION

Launched by Motorola freescale semiconductor

eIntelligence - Innovation Disclosure

Disclosure SC11244ZC (10428)

ID: SC11244ZC (10428)
Title: M3: Motorola MisMatch Calculator

Innovators: Cyndi RECKER, Patrick DRENNAN
Status: Reviewed
Submitted Date:
Review Date:
Sector: SPS
Patent Committee: Phoenix/SPS - Circuits
Business Unit: Analog Mixed Signal Technology Center
Organization:
Department: RS562
Location:
Submit Country: USA

Workflow

Role	Name	Action
First Innovator	Cyndi Recker	Complete
Co-Innovator	Patrick Drennan	Complete
Witness	John Bates Jr	Acknowledgement Complete Notebook Signed
Witness	Marco L Perez	Acknowledgement Complete Notebook Signed
Manager	Colin McAndrew	Acknowledgement Complete

Documents

Document Name	Description	Document Type	Uploaded By	Uploaded Date	Size

m3descrip.pdf Unspecified 7.9 Kb

Description

Name of Innovation or Engineering Development?
M3: Motorola MisMatch Calculator

What is the problem(s) to be resolved by or need(s) for your idea?
Mismatch (or matching) is a classic problem in analog circuit design. Most analog circuit blocks leverage the differential performance of devices that are in close proximity on the same chip to obtain high performance circuitry. The differential performance is mismatch. Mismatch directly affects the parametric yield loss of analog parts, and for some analog circuits, the mismatch directly determines the critical circuit performance such as bit resolution on high speed data converters.

The innovation presented here is a web-based mismatch calculator tool that allows the designer to input bias and geometry conditions for the matched pair and reports the input and output mismatch where appropriate. See attachment

Is your idea known or has it been disclosed outside of Motorola without a duty of confidence (e.g., non-disclosure agreement, joint development agreement, etc.)?
NO

Has a product incorporating your idea been sold, offered for sale, placed in production, qualification, sampled, described in any publication (including Motorola promotional literature), marketed, shipped to anyone outside of Motorola (customer or distributor), or placed into inventory?
YES, on

What is the earliest verifiable date that you communicated your idea to an individual that is NOT an innovator (e.g., the date a non-innovator witness signed your engineering notebook)?

Was your idea created or developed through work performed with a consortium, alliance, government contract, university, or joint venture?
NO

Please specify the Export Control Classification Number(s) (ECCN) to which this disclosure pertains
Unknown

Keywords

None Selected

Key Technologies

None Selected

[redacted]

Cynthia L Recker (Cyndi)

The address and personal information for this innovator should be treated as confidential.

Commerce ID:	10046392	**Core ID:**	RP0115
Phone:	+1(480)413-7546	**Fax:**	(480)413-4453
Email:	RP0115@email.mot.com		
Department:	RS562	**Location:**	
Mail Drop:	EL714	**Manager:**	COLIN C MCANDREW
Sector:	SPS	**Business Unit:**	Analog Mixed Signal Technology Center
SSN:	367783638	**Citizenship:**	USA
Residential Address:	3819 E. Ivyglen Street Mesa, AZ 85205 USA	**Mailing Address:**	, USA

Patrick G Drennan

The address and personal information for this innovator should be treated as confidential.

Commerce ID:	10003245	**Core ID:**	RP00520
Phone:	(480)413-4935	**Fax:**	(480) 413-4034
Email:	RP00520@email.mot.com		
Department:	RS562	**Location:**	
Mail Drop:	EL701	**Manager:**	COLIN C MCANDREW
Sector:	SPS	**Business Unit:**	Analog Mixed Signal Technology Center
SSN:	065607299	**Citizenship:**	USA
Residential Address:	961 W. Juanita Ave. Gilbert, AZ 85233 USA	**Mailing Address:**	, USA

M3: Motorola Mismatch Calculator Description

Mismatch (or matching) is a classic problem in analog circuit design. Most analog circuit blocks leverage the differential performance of devices that are in close proximity on the same chip to obtain high performance circuitry. The differential performance is mismatch. Mismatch directly affects the parametric yield loss of analog parts, and for some analog circuits, the mismatch directly determines the critical circuit performance such as bit resolution on high speed data converters.

The innovation presented here is a web-based mismatch calculator tool that allows the designer to input bias and geometry conditions for the matched pair and reports the input and output mismatch where appropriate.

For MOSFETs and BJTs, three procedures are available. The Voltage Driven procedure allows the user to input the nodal voltages of the devices in the matched pair and reports Id (output) mismatch and Vgs (input) mismatch. The Current Mirror procedure allows the user to input the reference current and Vd on the output device and reports Id mismatch in two scenarios, with and without output conductance on the output device. The Differential Pair procedure allows the user to input the reference current and nominal Vd and reports Id mismatch and the Vgs mismatch.

The reporting of Vgs mismatch as a description of the input offset voltage is unique and innovative. Standard industry practice is to use Vt mismatch for the input offset voltage. Vgs mismatch is more accurate because it describes the dependence of the input offset voltage on bias and geometry conditions.

Results are displayed in tabular form. Included in the output table are the mismatch contributions from fundamental process and geometry parameters. This is a unique capability only available with the Motorola mismatch model and calculator. Not only does this provide mismatch process diagnostics for the technology developer but it also helps the designer better understand the mismatch problem and guides him/her to regions of better opportunity. We plan to add a feature to the software procedure that will allow the user to display the random components, the gradient components and the device sensitivities for each of the process and geometry parameters.

This tool allows for current driven and voltage driven mismatch simulations. For mismatch prediction, the bias and geometry conditions must be considered simultaneously. For example, on a MOSFET current mirror, the nominal gate voltage is dependent upon the geometry. This tool takes this in account, prior art does not.

This tool can accomodate dissimilar geometries by evaluating the mismatch contribution from both devices in the matched pair. Other tools assume the devices in the matched pair are identical. In this case, only one device in the matched pair is varied, assuming twice the variability on one device. This approach is faulty if the devices in the matched pair are not designed identically.

This tool can simulate mismatch for multiple devices in parallel and/or multiple devices in series. Other tools assume a simple pair of devices.

This tool can simulate the mismatch contributions from multiple device types in single circuit block. For example, an emitter degenerate pair contains both resistors and BJT pairs. The matching of both pairs needs to be considered simultaneously.

This tool allows for multiple bias conditions for a constant geometry. This is critical since the mismatch can vary considerable over the bias conditions which is typical of many matched circuits. Other approaches use single point solutions.

APPENDEX II

SC1244ZC

M3: Motorola Mismatch Calculator

- Mismatch is a leading cause of yield loss and a determining factor of circuit performance in analog, mixed-signal ICs.
- Motorola has developed a new mismatch model that accounts for variations in physical process parameters and is accurate over geometry and bias.
- The designer need quick, easy access to the new model.
- The model is complex and automation is required.

$$\sigma^2_{Id} = \sum_{J} (\partial I_d / \partial p_j)^2 \sigma^2_{pj}$$

Prior Art

- Prior art based on the simplistic Pelgrom model.
  - P. G. Drennan, C. C. McAndrew "A Comprehensive MOSFET Mismatch Model," 1999 IEEE IEDM.
- Does not have a proper physical foundation and has gross errors in mismatch prediction.
- Prior art can't handle non-traditional devices such as graded channel (GCMOS & halo) and power MOSFETs.
- Inferior commercial tool is available from BTA Technology.

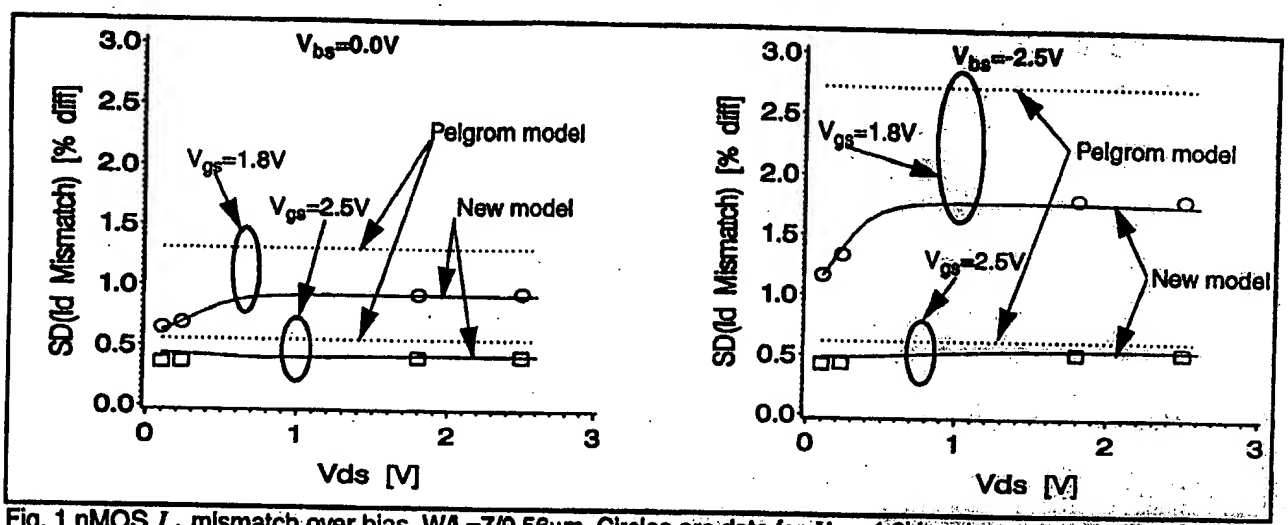


Fig. 1 nMOS I_d mismatch over bias, W/L=7/0.56µm. Circles are data for V_{gs}=1.8V and squares are for V_{gs}=2.5V.

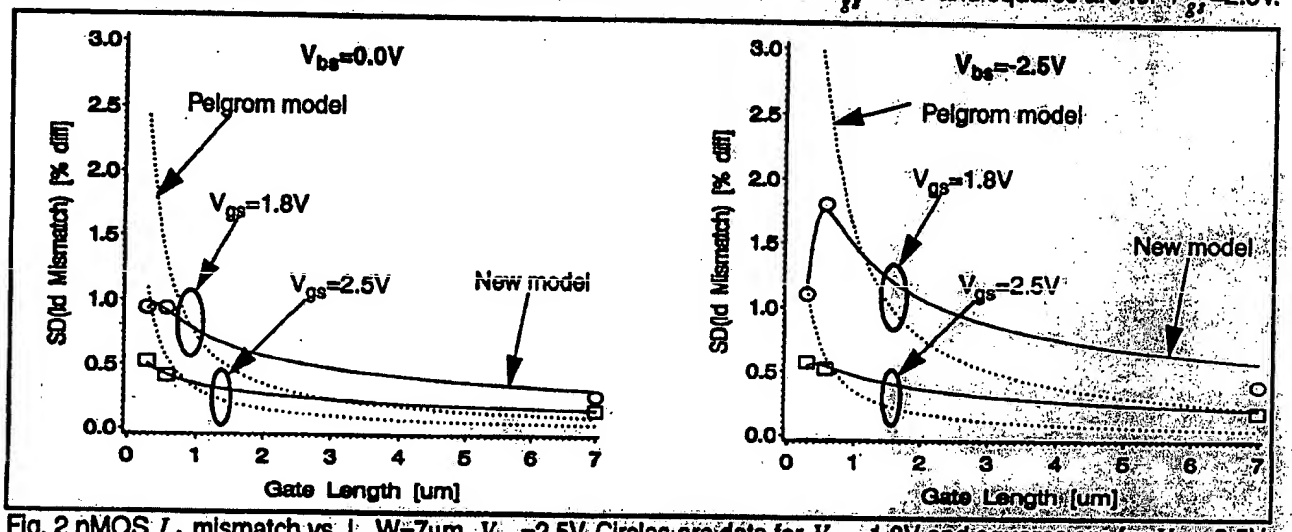


Fig. 2 nMOS I_d mismatch vs. L, W=7µm, V_{ds}=2.5V. Circles are data for V_{gs}=1.8V and squares are for V_{gs}=2.5V.

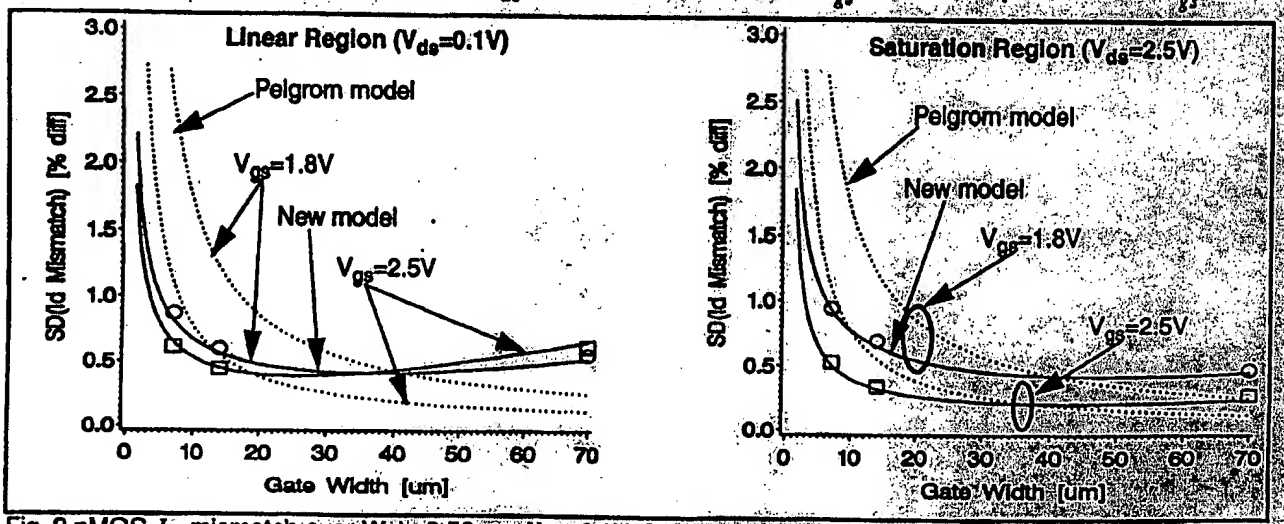
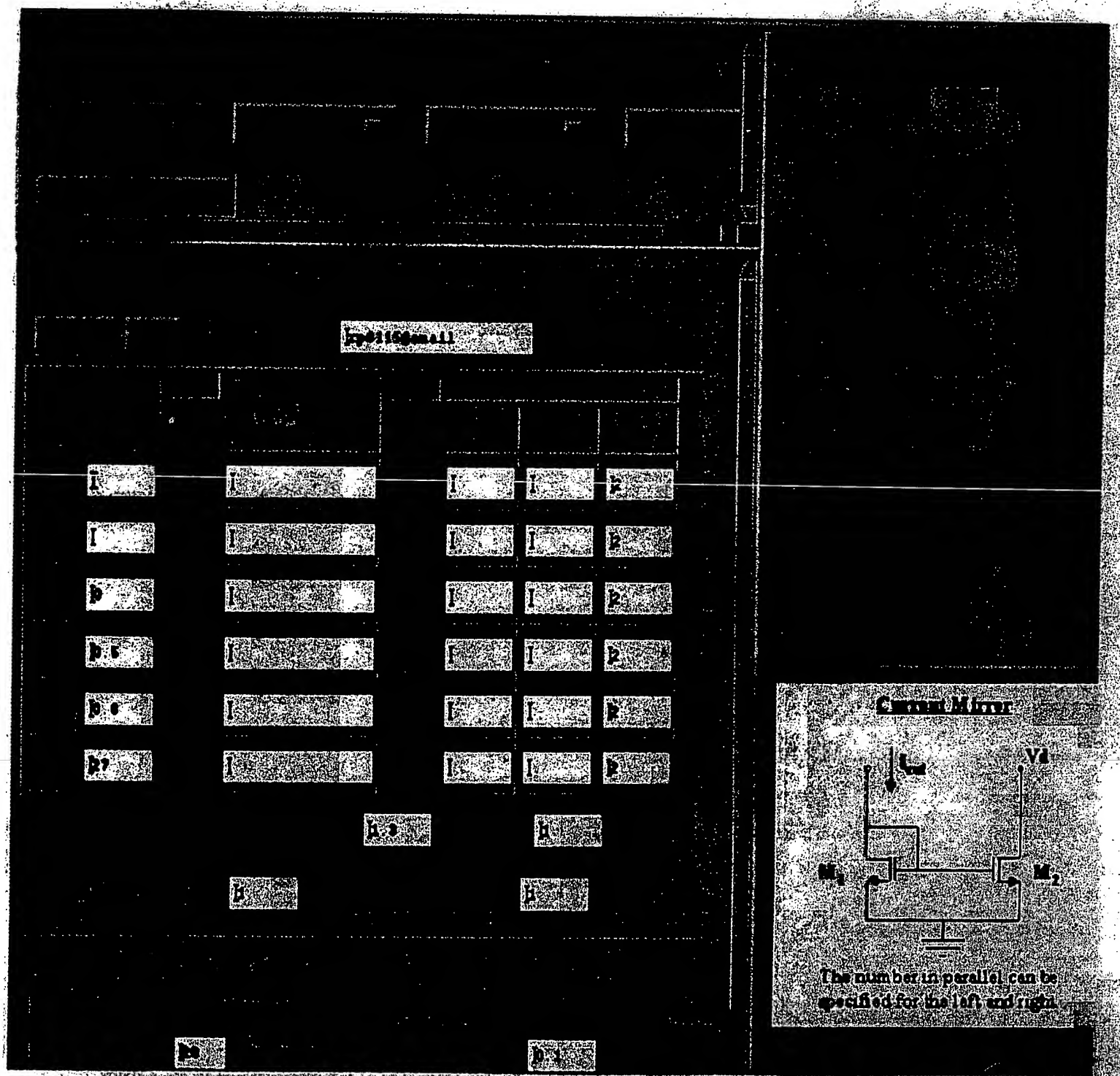


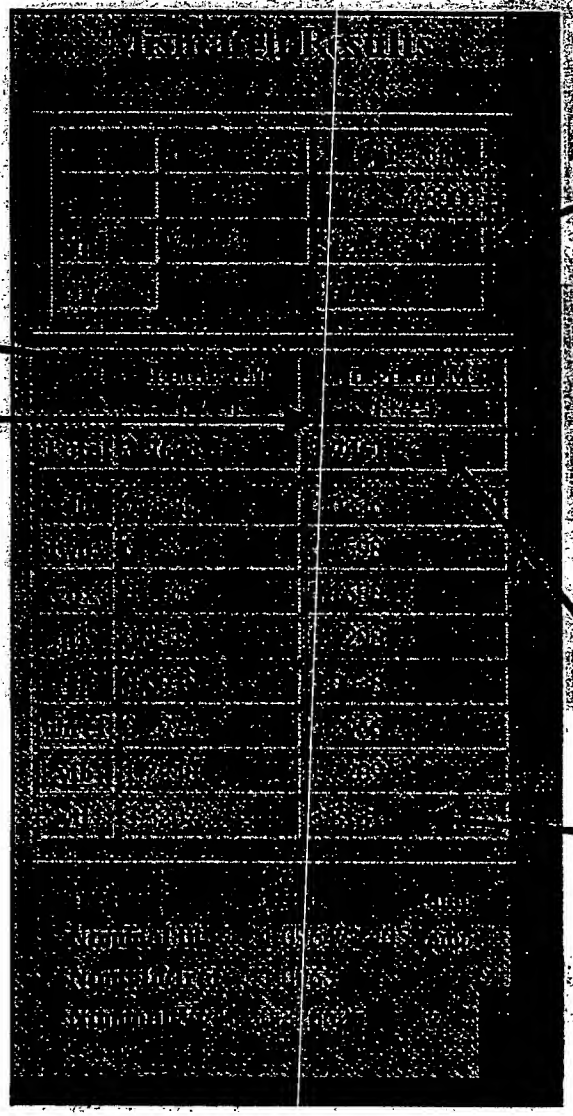
Fig. 3 nMOS I_d mismatch over W, L=0.56µm, V_{bs}=0.0V. Circles are data for V_{gs}=1.8V and squares are for V_{gs}=2.5V.

M3: Proposed Solution

- Automate the Motorola Mismatch Model in the form of a web-based tool
- Three different solution types
  - Current Mirror (for designers)
  - Differential Pair (for designers)
  - Voltage Driven (for technology developers)
- Make the tool readily available throughout Motorola and only to Motorola
- Perform single mismatch predictions
- Perform multiple mismatch predictions by allowing the designer to sweep over bias and geometry

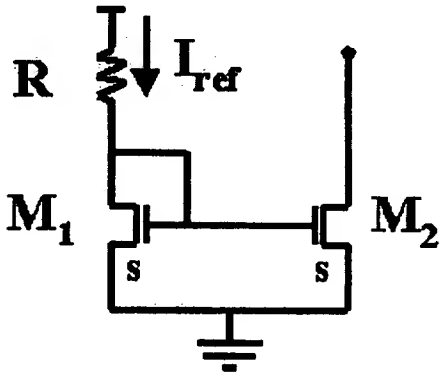

Current Mirror
The number in parallel can be specified for the left and right

Sample output

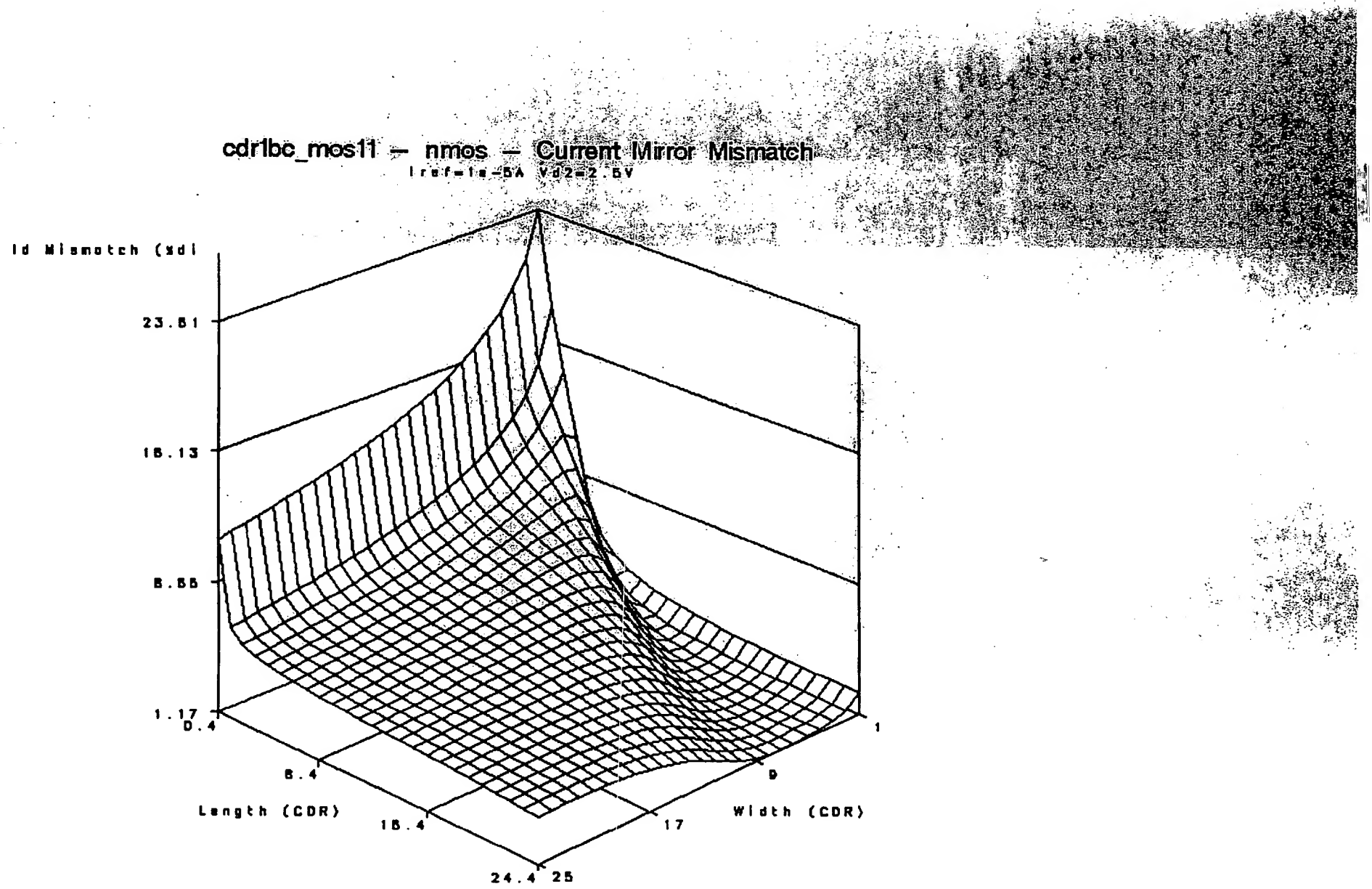


Data Entered into interface

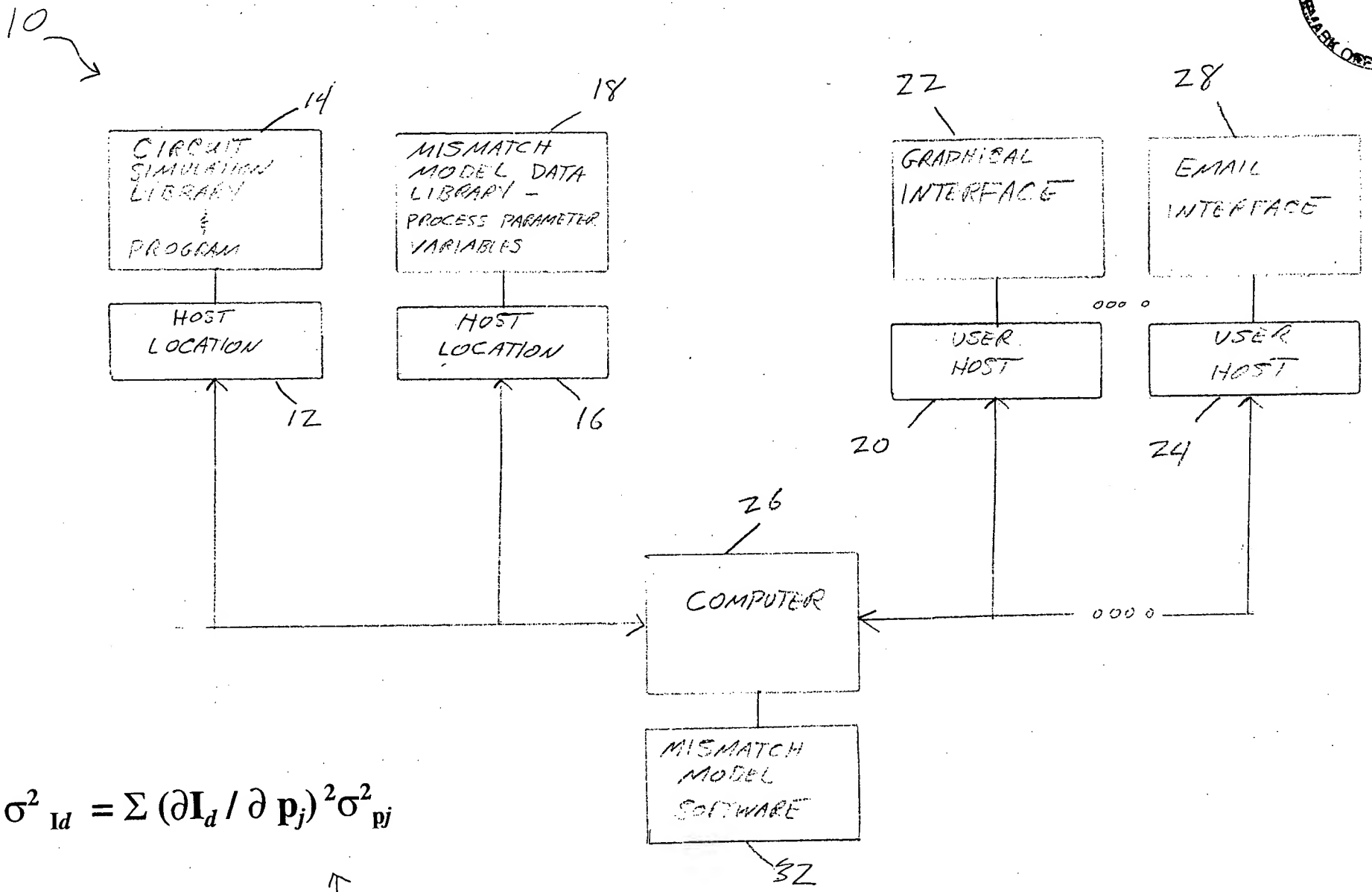
Two Outputs
- **Total Mismatch (%)**
- **Without go**
  Vd2 = Vg



Contributions to Mismatch
- **Root Sum of Squares, add variances, not standard deviations!**
- **vtl:Accounts for change in flat band voltage as a function of gate length**



All mismatches are given as 1-sigma standard deviations of sdiff in Id



$$\sigma^2_{Id} = \Sigma (\partial \mathbf{I}_d / \partial \mathbf{p}_j)^2 \sigma^2_{pj}$$

30

Fig. 1

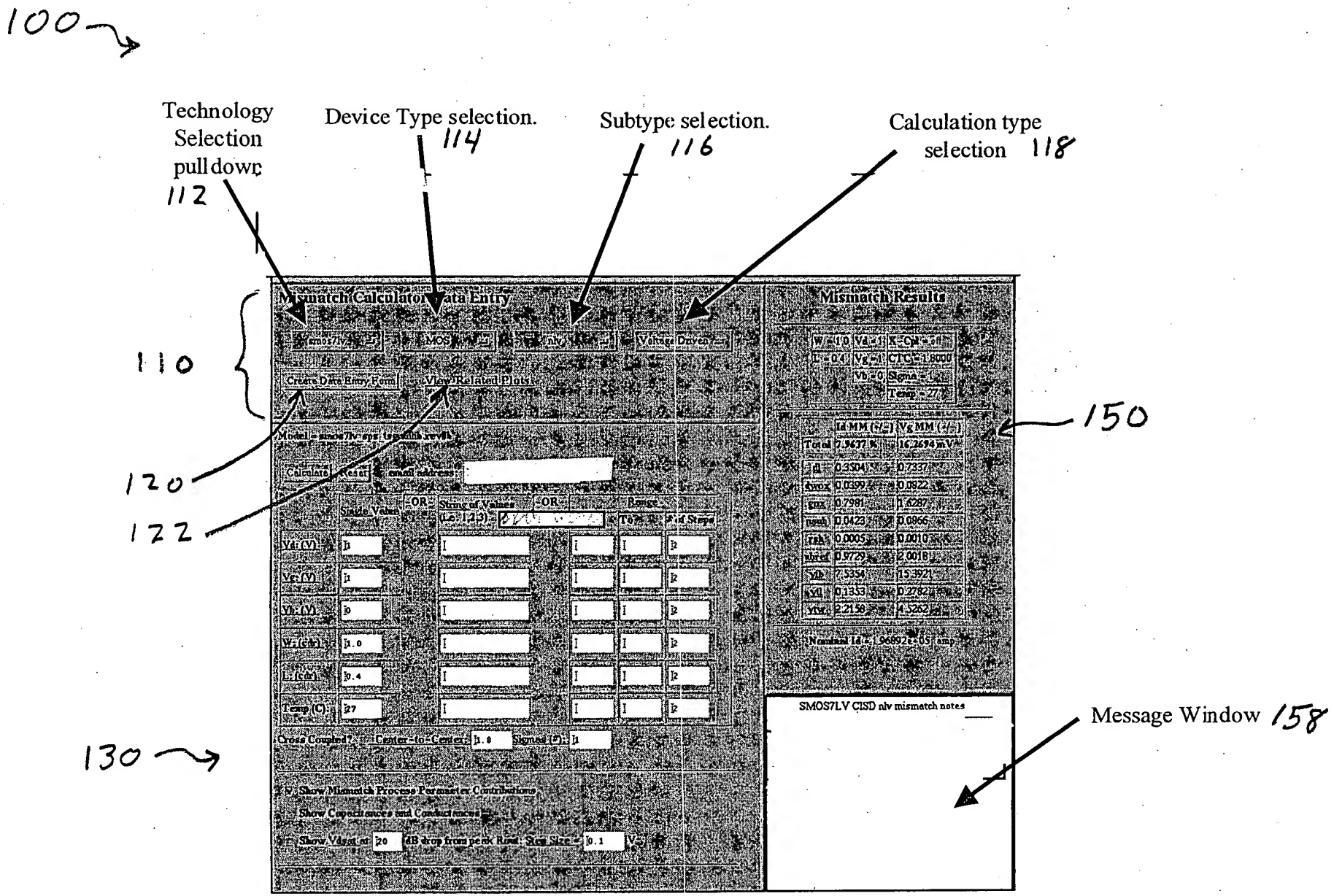

100
Technology Selection pull down
112
Device Type selection.
114
Subtype selection.
116
Calculation type selection
118
110
120
122
150
130
Message Window
158
Mismatch Calculator Data Entry
Mismatch Results
Create Data Entry Form
View Related Plots
Calculate
Reset
Single Value
String of Values
Range
SMOS7LV CISD nlv mismatch notes

Fig. 2

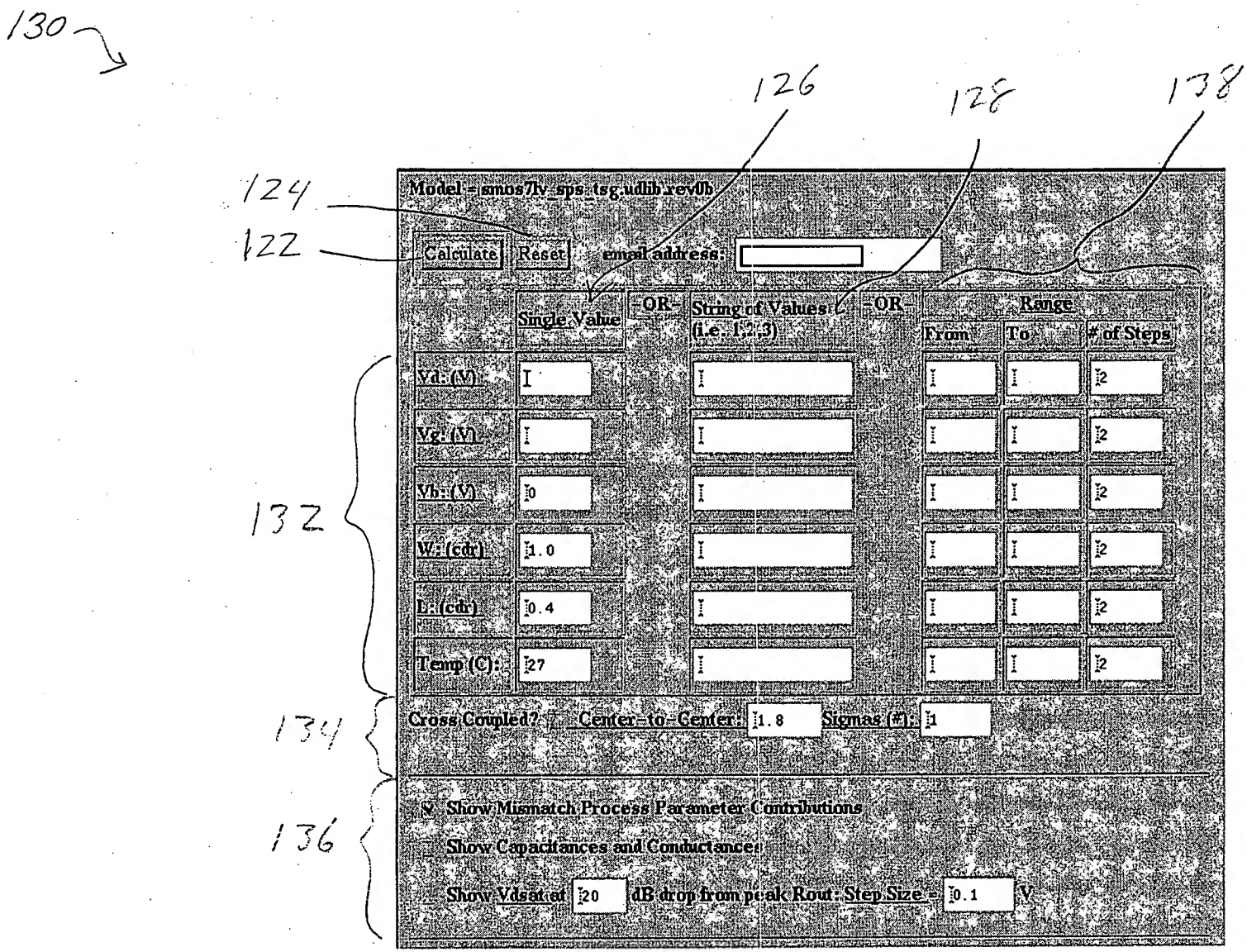

130
126
128
138
124
122
Model = smos7lv_sps_tsg.udlib.rev0b
Calculate
Reset
email address:
Single Value
-OR-
String of Values (i.e. 1,2,3)
-OR-
Range
From
To
# of Steps
Vd: (V)
Vg: (V)
Vb: (V)
W: (cdr)
L: (cdr)
Temp (C):
132
134
136
Cross Coupled?
Center-to-Center:
1.8
Sigmas (#):
Show Mismatch Process Parameter Contributions
Show Capacitances and Conductances
Show Vdsat at
dB drop from peak Rout. Step Size =
0.1
V

Fig. 3

Voltage Driven Output '

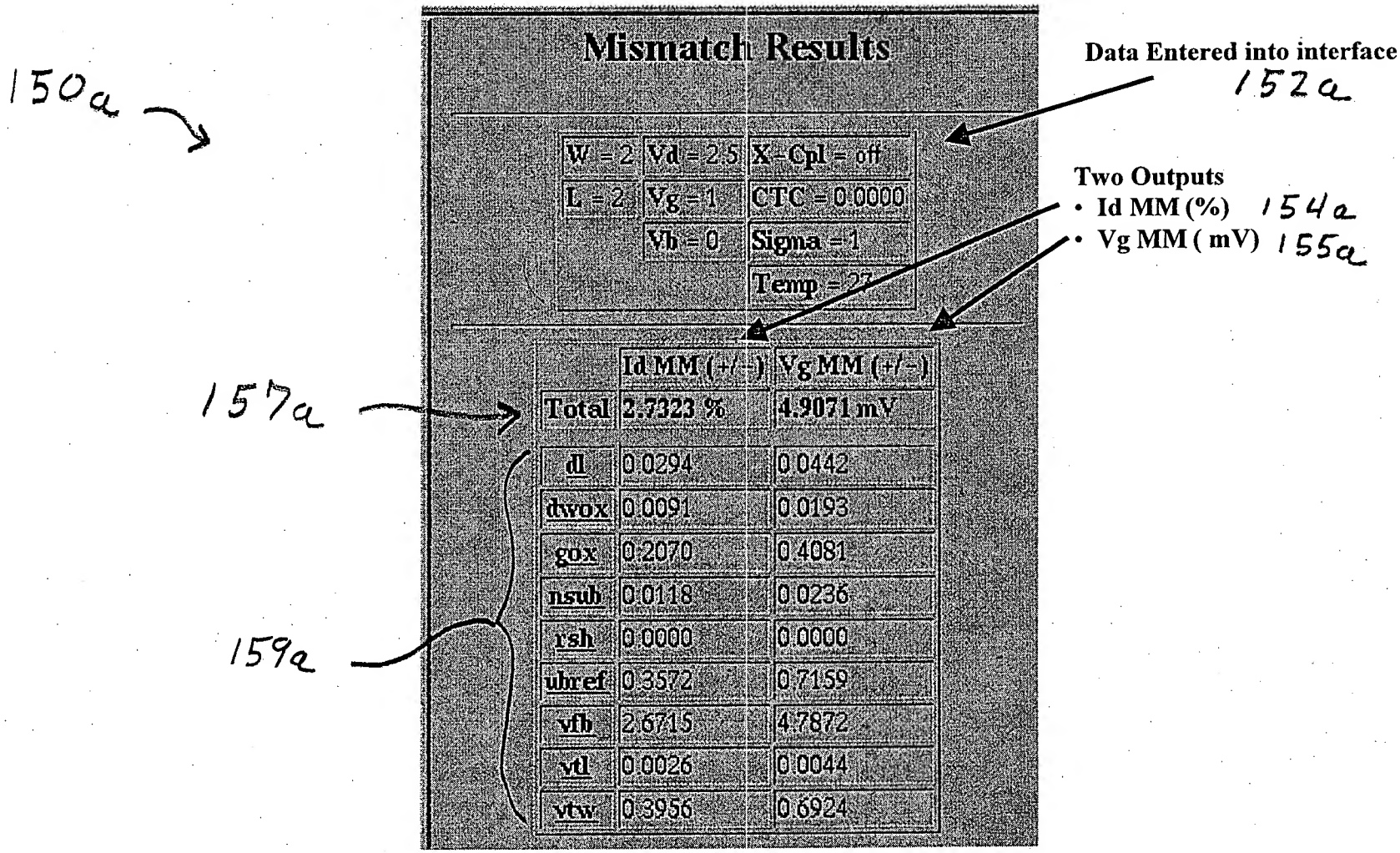


Fig. 4

Current Mirror Output

1506

Mismatch Results

1526

W = 4	Iref = 1e-5	X-Cpl = off
L = 4	Vd = 1.1	CTC = 4.8000
Np1 = 1	Vb = 0	Sigma = 1
Np2 = 1		Temp = 27

- Total Mismatch (%) 1546
- Without go Vd2 = Vg 1556

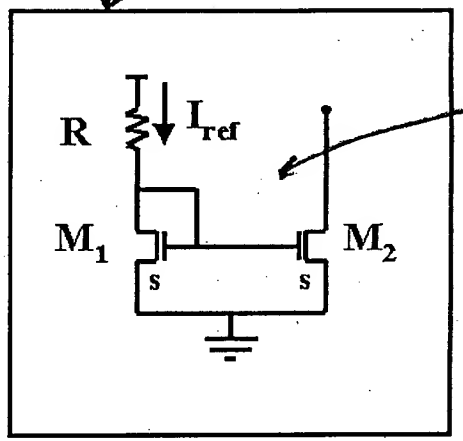
	Total MM (+/-)	w/o go on M2 (+/-)
Total	3.7633 %	3.7461 %
dl	0.0330	0.0326
dwox	0.1597	0.1598
gox	0.1669	0.1680
nl	0.1314	0.1298
rsh	0.0039	0.0038
ubref	0.2974	0.2966
vfb	1.7248	1.7209
vtl	3.3207	3.3131

1576

1596

Iref = 1e-5 amp
Nominal Id = 1.09647e-05 amp
Nom_Id/Iref = 1.0965
Nominal Vg = 0.326625 v

158



158a

Fig 5

DIFFERENTIAL PAIR OUTPUT

150c

Mismatch Results

W = 1.0	Iref = -10e-06	X-Cpl = off
L = 1	Vd = -1	CTC = 1.8000
Np = 1	Vb = 0	Sigma = 1
		Temp = 27

152c

Two Outputs
- Id MM (%) 154c
- Vg MM (mV) 155c

	Id MM (+/-)	Vg MM (+/-)
Total	3.2060 %	10.7680 mV
dl	0.3814	1.2847
dwox	0.0701	0.2318
gox	0.3942	1.3314
nsub	0.2671	0.8961
rsh	0.0002	0.0009
uhref	1.0403	3.4466
vfb	2.9558	9.9430
vtl	0.2861	0.9631
vtw	0.0006	0.0019

157c

159c

158

158b

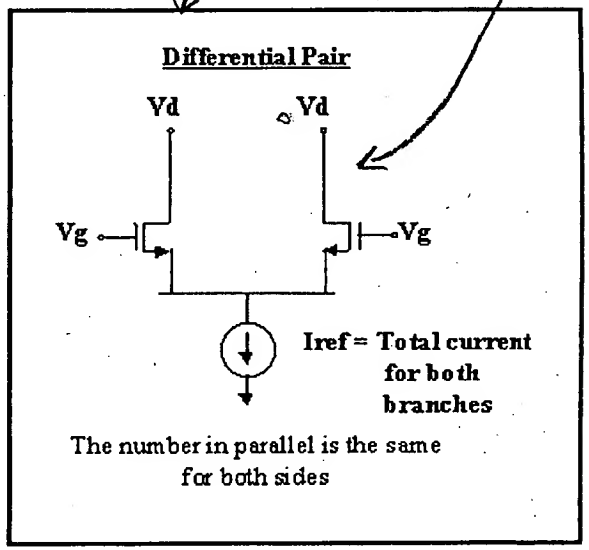


Fig. 6

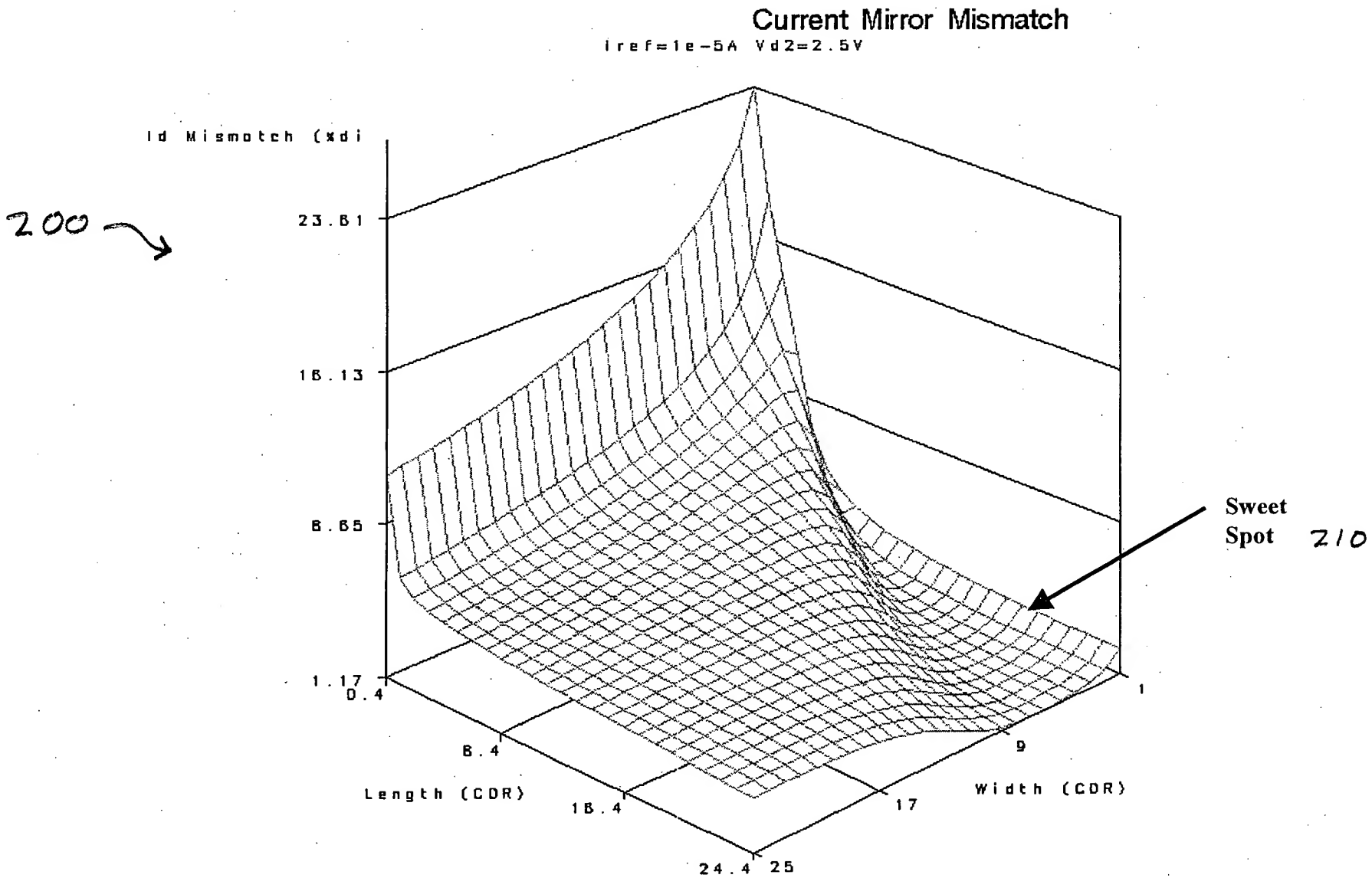

Current Mirror Mismatch
Iref=1e-5A Vd2=2.5V
Id Mismotch (%di
200
23.61
16.13
8.65
1.17
0.4
8.4
16.4
24.4
25
Length (CDR)
17
9
1
Width (CDR)
Sweet
Spot
210

Fig. 7

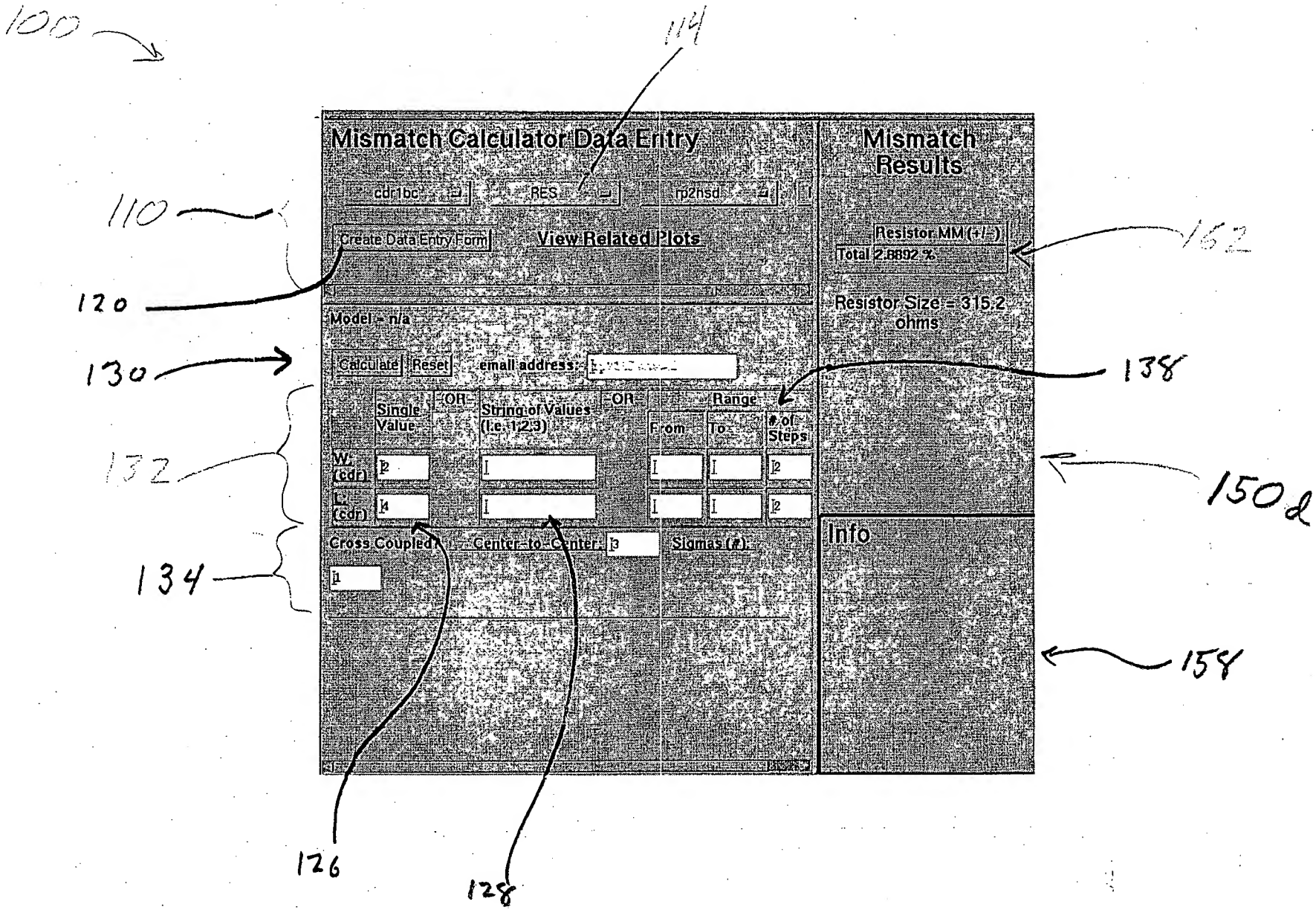

100
114
110
120
130
132
134
126
128
152
138
150d
154
Mismatch Calculator Data Entry
cdr1bc
RES
rp2nsd
Create Data Entry Form
View Related Plots
Model = n/a
Calculate
Reset
email address:
Single Value
-OR-
String of Values (i.e.1;2;3)
-OR-
Range
From
To
# of Steps
W (cdr)
L (cdr)
Cross Coupled
Center-to-Center
Sigmas (#):
Mismatch Results
Resistor MM (+/-)
Total 2.8892 %
Resistor Size = 315.2 ohms
Info

Fig. 8

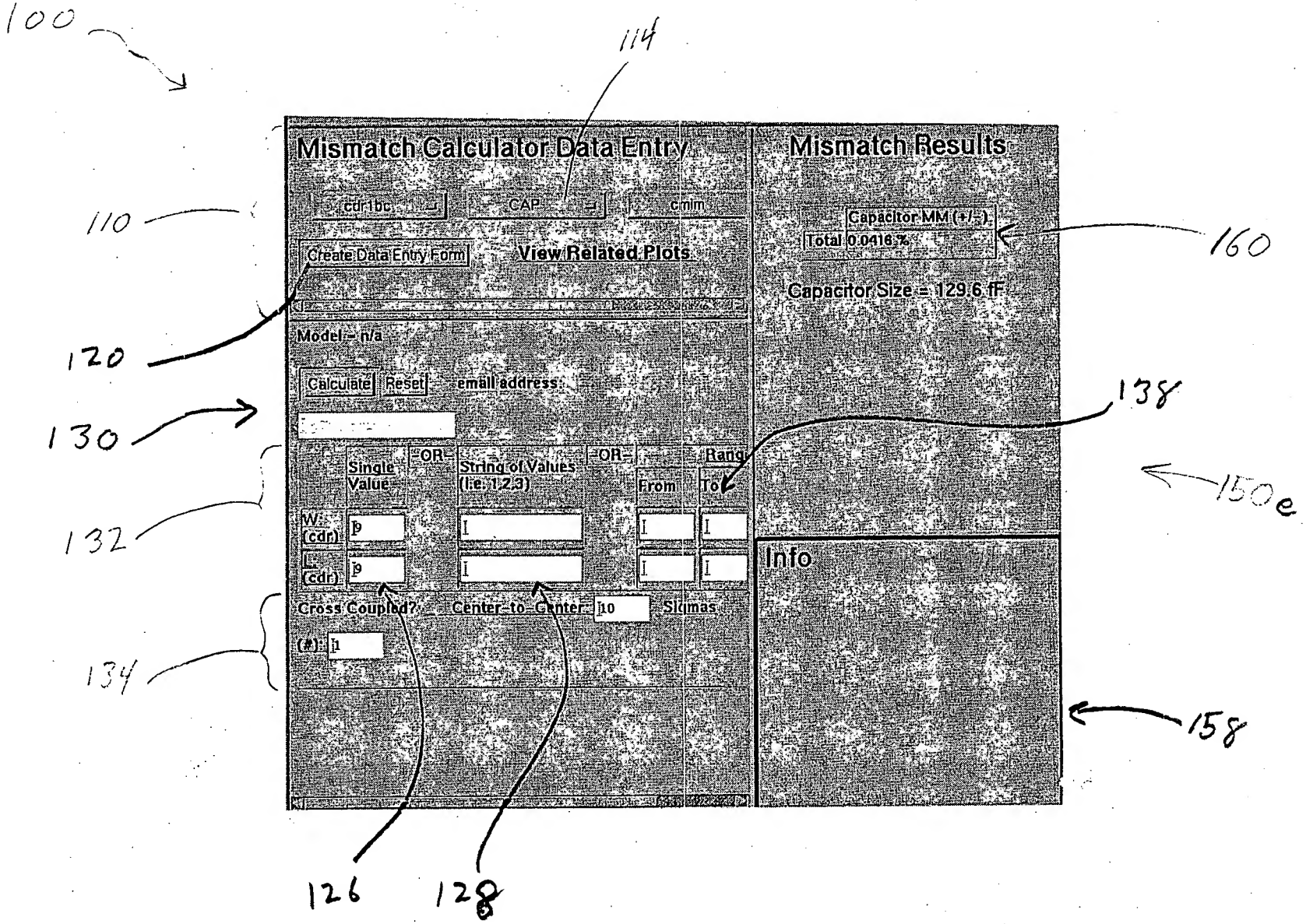

100
114
110
120
130
132
134
126
128
138
150e
160
158
Mismatch Calculator Data Entry
cdr1bc
CAP
cmim
Create Data Entry Form
View Related Plots
Model= n/a
Calculate
Reset
email address:
Single Value
-OR-
String of Values (i.e. 1,2,3)
-OR-
From
To
W: (cdr)
L: (cdr)
Cross Coupled?
Center-to-Center
10
Sigmas
(#):
1
Mismatch Results
Capacitor MM (+/-)
Total 0.0416 %
Capacitor Size = 129.6 fF
Info

Fig. 9

APPENDIX III

Specializing in:
Patents, Trademarks & Copyrights
& Corporate Matters

Harry M. Weiss* **Farley I. Weiss**
Jeffrey L. Weiss* **Mark H. Weiss**
Jeffrey D. Moy* **Craig R. Weiss**
Paul W. Davis*
**Registered Patent Attorney*

Of Counsel:
Karen J. Sepura
Jessica J. Weiss

Patent Engineer:
Matthew P. Schmehl

WEISS & MOY, P.C.
Attorneys and Counsellors
4204 N. Brown Ave.
Scottsdale, Arizona 85251-3914
(480) 994-8888
Fax (480) 947-2663

E-Mail Address: patents@weissiplaw.com

GOOD IDEAS NEED PROTECTION

Las Vegas, Nevada Office
5851 W. Charleston
Las Vegas, Nevada 89146
(702) 878-7323
Fax (702) 878-4510

Our Ref. MOT11244
Your Ref.

August 22, 2000

Cynthia L. Recker
Patrick G. Drennan
2100 E. Elliot Road
MD EL-714
Tempe, AZ 85284

Re: U.S. Patent Application Entitled -
"MISMATCH MODELING TOOL"

Dear Cindy and Pat:

Enclosed please find a copy of the above identified patent application revised as per your suggestions.

Kindly review the subject patent application as soon as possible and let us know if any additional changes are to be made or if the patent application is acceptable without change.

If you have any questions, please feel free to contact our offices.

Very truly yours,

WEISS & MOY, P.C.

Jeffrey D. Moy

JDM/wp
enclosures

cc: Charles Bethards

APP III

MISMATCH MODELING TOOL

Field of the Invention

This invention relates to mismatch models, and more particularly, to a mismatch calculator tool for predicting transistor, resistor and capacitor mismatch over bias, geometry, and layout conditions.

Background of the Invention

Mismatch is a leading cause of yield loss and a determining factor of circuit performance in analog, mixed-signal (AMS) ICs. A new method of modeling mismatch that accounts for variations in physical process parameters and is accurate over geometry and bias has been developed. However, as with prior mismatch models, the use of this new mismatch model required intensive manual calculations thus making it non-user friendly. Therefore, the application of the new mismatch methodology, or model, has been combined with computer programming and electronic circuit simulation and modeling resulting in a mismatch tool. Thus, users of the mismatch tool, such as designers and other engineering professionals, can create more robust designs by quickly evaluating the mismatch opportunity in a fraction of the time that the manual calculations required and

with more accuracy. The mismatch tool further allows the designer to simulate a variety of bias and geometry conditions in a matter of seconds, including providing batch-mode capability to perform multiple sweeps over bias and geometry to aid in finding a desired configuration.

Brief Description of the Drawings

Fig. 1 is a simplified functional block diagram of the mismatch modeling tool in an embodiment of the present invention;

Fig. 2 is an example of an interface to the mismatch modeling tool in an embodiment of the present invention;

Fig. 3 is a data entry input frame of the interface shown in Fig. 2;

Fig. 4 is a mismatch results output frame of the interface shown in Fig. 2 for the voltage driven scenario;

Fig. 5 is a mismatch results output frame of the interface shown in Fig. 2 for the current mirror scenario;

Fig. 6 is a mismatch results output frame of the interface shown in Fig. 2 for the differential pair scenario;

Fig. 7 shows an example of a mismatch results three dimensional output plot showing a sweet spot in a plot of Id versus geometry for an nmos current mirror;

Fig. 8 is the interface screen of Fig. 2 showing the data entry input frame and mismatch results output frame for a resistor mismatch calculation scenario;

Fig. 9 is the interface screen of Fig. 2 showing the data entry input frame and mismatch results output frame for a capacitor mismatch calculation scenario.

Detailed Description of the Drawings

Referring to Fig. 1, a simplified functional block diagram of a mismatch modeling tool 10 in an embodiment of the present invention is shown (the "mismatch tool 10" hereinafter). The mismatch tool 10 comprises the mismatch model $\sigma^2_{Id} = \Sigma (\partial I_d/\partial p_j)^2 \sigma^2_{pj}$ ("mismatch model 30" hereinafter). The derivation and explanation of the mismatch model 30 is contained within the paper A Comprehensive MOSFET Mismatch Model by P. Drennan and C. McAndrew, IEEE ICMTS, 2000 ("Drennan et al." hereinafter), the contents of which are incorporated herein by reference. Further explanation of the model is contained within Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design, - Ph.D. dissertation, Arizona State University, May 1999, by P. Drennan ("Drennan" hereinafter) which is also incorporated herein by reference.

Referring again to Fig. 1, the mismatch tool 10 further comprises the mismatch model software 32, which is run upon a computer, or server, 26. The computer 26 is electronically connected to a circuit simulation library and program 14. The circuit simulation library and program 14 may be comprised of any of the many electronic circuit modeling and simulation packages available. Some examples include the SPICE program developed by the University of California - Berkeley, but may also include PSPICE, MCSPICE, Saber, SmartSpice, etc. The circuit simulation library and program 14 is stored, and may be executed, at a host location 12. The host location 12 may be integral to the computer 26, or may also represent an unrelated computer or storage location. The mismatch tool 10 further comprises mismatch model data libraries 18, stored within a host location 16. The mismatch model data libraries 18 comprise process parameter variables used within the model 30 to account for the physical parameters affecting mismatch. As in the previous case, the host location 16 may be storage within, or part of, the computer 26, or may also represent an unrelated computer or storage location.

The mismatch tool 10 further comprises the data input and data output interfaces that may be comprised of any data interface method or system. In an embodiment of the present invention, a web based application is utilized. A web based

application is an application that is downloaded from a computer network each time the application is run. The computer network may be either an in-house local area network, or intranet, or a large scale wide area network, or internet. The advantage is that the application can be run from any computer, either on a local area network or via a wide area network such as the world wide web, and the software is routinely upgraded and maintained by the hosting organization rather than each individual user. Additionally, the web based applications are not limited to conventional web browser applications such as Netscape. Other web based application systems or programs may be employed within the web based application concept without departing from the spirit or scope of the present invention.

In an embodiment of the present invention, a graphical interface 22 is presented upon a user host 20. The user host 20 may be a standalone computer, a time shared computer terminal, etc. Furthermore, an email interface 28 may also reside upon a user host 24, which again may be a standalone computer, a time shared computer terminal, etc. The use of an email interface 28 upon a separate host 24, connected electronically to the computer 26, allows remote users to submit and receive data from locations remote from the computer 26, including globally. The automated combination of the mismatch model 30, the mismatch model software 32, the circuit simulation library and program

14, and the mismatch model data libraries 18, gives users a significant advantage in achieving reduced cycle time for design and improved product quality through more robust designs.

The mismatch tool 10 in an embodiment of the present invention further comprises a plurality of different calculation scenarios: a Voltage Driven scenario, a Current Mirror scenario, and a Differential Pair scenario, for MOSFET and BJT transistor devices; and a resistor calculation scenario and capacitor calculation scenario. Each of these calculation scenarios can be combined with calculations for other analog design objectives. Those skilled in the art will recognize that additional calculation scenarios than these five are possible, and are also within the spirit and scope of an embodiment of the present invention. The five scenarios above are presented as examples of scenarios popular with those skilled in the art.

Referring to Fig. 2, an example of an interface to the mismatch tool 10 in an embodiment of the present invention is shown. The interface screen 100 comprises three major areas, or frames, in an embodiment of the present invention. The frames of the interface screen 100 comprise a calculation setup frame 110, a data input frame 130, and a data output frame 150. The data output frame 150 also comprises a message frame 158.

The frames of the interface screen 100 provide a user with the means to input data and receive returned output data in a

graphical user friendly format. The user is guided through a sequence of pulldown menus within the calculation setup frame 110, wherein the user is presented with a technology selection 112, a device type selection 114, a subtype selection 116 and a calculation type selection 118. Each of the pulldown menus is actively generated, using programming languages such as JavaScript, Perl, etc., based upon the preceding menu selections.

As new technologies are developed and added into an embodiment of the present invention, the programming and database libraries are modified to include data files comprising the added technology name along with its shrink factor and design unit information. These programming modifications make the technology available on the pull down menus in the calculation setup frame 110. Additionally, a technology directory (not shown herein) is also created that comprises the device types available for analysis. Included in this technology directory is an electronic circuit / component model file for insertion into the circuit simulation library and program 14 that is used for the simulations along with files of measured data to be used in the calculation for the variance and gradient terms, and new model data to be added into the mismatch model data libraries 18. The aforementioned programming changes

may be accomplished in a variety of methods by those skilled in the art.

The calculation setup frame 110 further comprises a View Related Plots 122 button, or link, that will launch a second graphical displaying a page that contains mismatch measured data, playback plots, and 3D and contour plots of the device mismatch over geometry, such as the 3D plot of Current Mirror mismatch versus geometry in Fig. 7. These plots help guide the user to opportunities for better mismatch, such as the sweet spot shown on the right side of Fig. 7, that may otherwise not be apparent from single point solutions calculated in the mismatch tool 10.

Following the selection of the desired technology in the calculation setup frame 110, the user selects a create data entry input form 120 button. This selection causes the data input frame 130 to be generated.

Referring to Fig. 3, a data entry input frame 130 of the interface of Fig. 2 is shown. In an example of an embodiment of the present invention, an electronic circuit simulation model file name, it's revision number, and such other information as desired, is displayed at the top of the data entry input frame 130. The data entry input frame 130 further comprises geometry, bias and temperature condition selection parameters 132 for the selected technology and device. The specific geometry, bias and

temperature condition parameters 132 that are generated following the selection of the create data entry input form 120 button are dependent upon the previous technology and device selections and therefore may vary. For example, the specific geometry, bias and temperature condition parameters 132 shown here in Fig. 3 result from the voltage driven scenario. However, additional or fewer fields may be generated for other scenarios, e.g. the current mirror and differential pair scenarios will also have a field, Np1, etc. to designate the number of devices placed in parallel. Those skilled in the art will be familiar with the bias and geometry condition parameters 132 displayed however. The user will next enter the desired bias, geometry and temperature values into the data entry fields reflecting the number of values desired for each parameter. The data entry fields are comprised of three columns: a single-value data entry column 126, a string-of-values data entry column 128, and range-of-value data entry column 138. Each of these data entry fields is utilized as follows. The single-value data entry column 126 accepts single values for each geometry, bias and temperature condition parameter. The string-of-values data entry column 128 accepts a delimited list of values for each geometry, bias and temperature condition parameter. The range-of-value data entry column 138 allow the user to input sweeps of

geometry, bias and temperature condition parameters by specifying the start, stop, and step values.

In an embodiment of the present invention, the desired values for each geometry, bias and temperature condition parameter may be entered into the single-value data entry column 126, the string-of-values data entry column 128, and the range-of-value data entry column 138 in any combination of the three columns. If multiple columns contain data entries for the same geometry, bias and temperature condition parameters, the calculation precedence is established from right to left (i.e. the range-of-value data entry column 138 supercedes the string-of-values data entry column 128 which in turn supercedes the single-value data entry column 126.

Additionally, if the data input frame 130 contains values only in the single-value data entry column 126, the output is directed to the data output frame 150 shown on the right side of Fig.2, as well as in Figs 4-6. If either the string-of-values data entry column 128, or the range-of-value data entry column 138 contains data, the output will be placed in a delimited text file (such as is suitable for importing into spreadsheet or word processing programs) and the user receives the results following the completion of the calculations. This feature is present since many applications, including web browsers such as Netscape, will time-out before the mismatch calculator 10 can

return the results from multiple calculations to the data output frame 150. Also, since the multiple calculations can require a period of time to run, this feature allows the user to continue with other tasks while the calculations are being run. The comma delimited text file data table can be used to generate mismatch plots such the one in Fig. 7, to build behavioral models, for use as a look-up table, to generate trend plots over bias, geometry or temperature, and to compare devices within and across technologies. Fig 7 shows an example of a mismatch results three dimensional output plot showing a sweet spot in a plot of Id versus geometry for an nmos current mirror.

An additional feature in an embodiment of the present invention is that each of the parameter names, as well as any other desired label, may be hypertext linked to a short description or definition.

It should be noted that in an embodiment of the present invention, the temperature condition parameter changes the operating temperature of the electronic circuit simulation package, such as SPICE, behind the mismatch tool 10 without the mismatch being measured and characterized over various temperatures. Changes in the temperature condition parameter will result in changes to the drain currents obtained from the SPICE simulation. In another embodiment of the present

invention however, the mismatch may be measured and characterized over various temperatures.

An additional feature in an embodiment of the present invention is active error checking that automatically checks all bias and geometry condition parameter data entry values entered into the input columns: single-value data entry column 126, string-of-values data entry column 128, and/or range-of-value data entry column 138.

Below the input columns for geometry, bias and temperature, the user can choose to simulate the mismatch pair in a cross-couple configuration by entering appropriate data values into cross-coupled configuration data entry fields 134 that are comprised of fields for Center-to-center and Sigmas(#). A cross-coupled pair is distinguished from a common centroid pair in that not all cross-coupled pairs are common centroid. That is, the effective center of the first device needs to be coincident with the effective center of the second device to be considered a common centroid pair.

In an embodiment of the present invention the user may also optionally select to show mismatch process parameter contributions, show capacitances, and show VdSat by selecting the appropriate Show Parameter checkboxes 136.

During the course of entering the above data, the user may rest all the fields to their default values by clicking on a reset button 124.

Once the user has entered all of the desired data input values, they then press a Calculate button 122. All of the user data that has been input into the data entry input frame 130 is collected and combined with information to form a SPICE or Mica type netlist. The netlist is run on the computer 26 and the results are parsed out to several variables. The simulation results are combined with the mismatch model 30 coefficients to perform the mismatch calculations. A further feature of an embodiment of the present invention is the ability of the mismatch tool 10, using the mismatch model 30, to predict the mismatch standard deviation of a radially dependent gradient. Radially dependent gradients may result from spin-coat processes such as photoresist and developer deposition, or other single wafer process steps such as etch or material deposition. In the presence of radially dependant gradients, the matched pair of devices on one side of a wafer may have a positive gradient offset, while the matched pair on the opposite side of the wafer has a negative gradient offset. The overall measured distribution will still be centered about zero in the presence of the radial gradient, but the dispersion will bloom. Radial based gradients can be eliminated by using common centroid

matched pairs. Thus, the mismatch tool 10 using the mismatch model 30, to predict the mismatch standard deviation of a radially dependent gradient is valid for common centroided pairs.

Referring again to Fig. 2, it will be recalled that the user is presented with the calculation type selection 118. This selection features five of the most popular types of calculation scenarios for MOSFET and BJT transistors, resistors and capacitors as follows:

Voltage Driven Scenario

The Voltage Driven scenario was developed primarily for characterization and technology development engineers. The entries for the Voltage Driven configuration entries into the calculation type selection 118 comprise: Vd - drain voltage; Vg - gate voltage; Vb - bulk; W - Width; and L - Length as are shown in the entered data frame 152a.

Referring to Fig. 4, a data output frame 150a is shown. The data output frame 150a contains two columns of data. The Id mismatch 154a, presented in the left column, is given as a percent difference between two devices. The right column contains the Vg mismatch 155a, which is the input offset voltage.

The first row of output data is the total Id and Vg mismatch 157a, given as a one-sigma standard deviation number, although this is user definable. The (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution. A total mismatch is computed from the individual process parameter contributions listed in the remaining rows of data parameters 159a comprised of: dl - offset in polysilicon gate length; dwox - offset in active region width; gox - gate oxide thickness; nsub - substrate dopant concentration; rsh - source and drain sheet resistances; ubref - reference mobility; vfb - flatband voltage; vtl - modification of Vfb for short channel devices, and Vtw - accounts for changes in MOSFET narrow-width and inverse-narrow-width effects.

All process parameter contributions are given as one-sigma standard deviation numbers and these parameters are combined as a root-sum-of-squares to generate the total mismatch 157a (i.e. square each standard deviation to get a variance, add the variances, and square-root the total variance to the total standard deviation.) The user, by examining the data parameters 159a results that are presented in the data output frame 150a, will be able to determine the major contributors to the mismatch in a particular case. The user can then use this information to target those parameters that affect the mismatch.

Current Mirror Scenario

The Current Mirror mismatch scenario was developed primarily for analog and mixed-signal designers although many designers will find the mismatch tool 10 of value. The entries for the Current Mirror configuration entries into the calculation type selection 118 comprise: Vd - drain voltage; Vb - bulk; Iref - reference current; W - Width; and L - Length as are shown in the entered data frame 152b.

The Current Mirror scenario differs from the Voltage Driven scenario in that the user has the option of specifying the number of unit devices placed in parallel, Np1 and Np2, for both M_1 and M_2 through the use of an additional data entry field in the data input frame 130 (not shown in Fig. 2). This makes the mismatch tool 10 suitable for simulating the mismatch in the presence of ratioed mirrors. The variances across each of the unit devices, in a grouping of parallel devices, add to give the total variance. But, the overall sensitivity of the mirror to each unit device is reduced, thereby giving an overall reduction in mismatch when multiple devices are placed in parallel.

An example mismatch tool 10 output frame 150b, contains two columns of data, the total mismatch, Total mismatch 154b, and the mismatch without the output conductance, go, on M_2, w/o go on M2 155b. In the latter case, w/o go on M2 155b, the mismatch simulation is performed with the drain of M_2 tied to the gate. In

this manner, the mismatch results can be added to a SPICE TYPE circuit netlist without double counting the effect of the output conductance on M_2.

A total mismatch is computed from the individual process parameter contributions listed in the remaining rows of data parameters 159b comprised of: dl - offset in polysilicon gate length; dwox - offset in active region width; gox - gate oxide thickness; nl - substrate dopant concentration; rsh - source and drain sheet resistances; ubref - reference mobility; vfb - flatband voltage; and vtl - modification of Vfb for short channel devices.

As in the voltage driven scenario, all process parameter contributions are given as one-sigma standard deviation numbers, that may be user defined to other than one-sigma, and these parameters are combined as a root-sum-of-squares to generate the total mismatch 157b. The user, by examining the data parameters 159b results that are presented in the data output frame 150b, will be able to determine the major contributors to the mismatch in a particular case. The user can then use this information to target those parameters that affect the mismatch.

Since Current Mirrors are often operated over a range of current, the mismatch can change dramatically over the operating region of the matched pair (approximately 5X in this case). The

mismatch tool 10 allows the user to sweep the bias conditions to check the mismatch over the anticipated operating region.

Note that Vg mismatch is not provided for the Current Mirror case since the gates of M_1 and M_2 are tied together and cannot be offset. For this requirement, the current driven, Differential Pair scenario is suggested.

Differential Pair Scenario

The Differential Pair scenario was also developed primarily for analog and mixed-signal designers although again many designers will find the mismatch tool 10 of value. The Differential Pair scenario is nearly identical to the Voltage Driven scenario with the exception that the MOSFET matched pair is current driven. The entries for the Differential Pair configuration entries into the calculation type selection 118 comprise: Iref - reference current (Iref for the Differential Pair is the current for both branches; Data Entered into interface for p-type must be entered as a negative i.e. -10u); Vd - drain voltage; Vb - bulk; W - Width; and L - Length as are shown in the entered data frame 152c. An additional data entry field in the data input frame 130 (not shown in Fig. 2) allows the user to change the number of devices placed in parallel which is required to be the same for both the left and right devices.

Referring to Fig. 6, a differential pair scenario assumes a particular circuit. As an aide to the user, the message frame158 will display that circuit. Thus - message frame 158 shows a picture of the assumed circuit 158b.

Referring further to Fig. 6, the data output frame 150c is shown. The data output frame 150c contains two columns of data. The Id mismatch 154c, presented in the left column, is given as a percent difference between two devices. The right column contains the Vg mismatch 155c, which is the input offset voltage.

The first row of output data is the total Id and Vg mismatch 157c, again, given as a one-sigma standard deviation number that may be user defined to other than one-sigma. The (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution. A total mismatch is computed from the individual process parameter contributions listed in the remaining rows of data parameters 159c comprised of: dl - offset in polysilicon gate length; dwox - offset in active region width; gox - gate oxide thickness; nsub - substrate dopant concentration; rsh - source and drain sheet resistances; ubref - reference mobility; vfb - flatband voltage; vtl - modification of Vfb for short channel devices, and Vtw - accounts for changes in MOSFET narrow-width and inverse-narrow-width effects.

The user, by examining the data parameters 159c results that are presented in the data output frame 150c, will be able to determine the major contributors to the mismatch in a particular case. The user can then use this information to target those parameters that affect the mismatch.

Referring to Fig. 7, an example of a mismatch results three dimensional output plot showing a sweet spot in a plot of Id versus geometry for an nmos current mirror ("output plot 200" hereinafter) is shown. The example output plot 200 shows the results of a spread or range of calculations such as would have been input into the string-of-values data entry column 128 or the range-of-value data entry column 138. Thus - the user when presented with an output plot 200 as shown can immediately discern the sweet spot 210.

Mismatch variance is not the only design objective for a matched pair of devices. Thus - an embodiment of the present invention has as further features the addition of several parameter calculations to the mismatch tool 10 to allow simultaneous monitoring of multiple criteria. With every circuit configuration, as previously discussed, the nominal Id is provided. For the Current Mirror and the Differential Pair scenarios of Fig. 5 and 6, the nominal Vg, is provided and the Current Mirror scenario output reports Id/I ref.

Resistor Scenario

Referring to Fig. 8, an interface screen showing the data entry input frame and mismatch results output frame for a resistor mismatch calculation scenario is shown. The interface screen 100, as previously discussed, comprises a calculation setup frame 110, a data input frame 130, a data output frame 150, and a message frame 158. In the resistor calculation scenario in an embodiment of the present invention, the user will select a device type selection 114 designating a resistor (abbreviated "RES" in Fig. 8. Following completion of the selections of the desired technology and the create data entry input form 120 button in the calculation setup frame 110, the data input frame 130 is generated.

The data entry input frame 130 comprises length and width selection parameters 132. The specific length and width parameters 132 that are generated following the selection of the create data entry input form 120 button are dependent upon the previous technology and device selections and therefore may vary. As previously discussed, the desired values for the width and length parameters may be entered into the single-value data entry column 126, the string-of-values data entry column 128, and the range-of-value data entry column 138 in any combination of the three columns. And as before, if multiple columns contain data entries for the same width and length parameters,

the calculation precedence is established from right to left (i.e. the range-of-value data entry column 138 supercedes the string-of-values data entry column 128 which in turn supercedes the single-value data entry column 126.

Below the input columns for width and length, the user can choose to simulate the mismatch pair in a cross-couple configuration by entering appropriate data values into cross-coupled configuration data entry fields 134 that are comprised of fields for Center-to-center and Sigmas(#). It should be noted that the process for computing the mismatch is a little different for the resistor scenario then that of the transistor scenarios. The primary difference is that a SPICE or MCSPICE type program is not utilized as the calculation is much simpler. Instead, a parameter file is used for the measured data terms.

An additional difference is the equation for computing the mismatch. The computational code for this mismatch calculation is: $(\sigma_R^2/R^2) = (\sigma_L^2/L^2) + (\sigma_w^2/W^2) + (\sigma_{LW}^2/LW) + (g*ctc^2)$.

Following the calculation of the resistor scenario, if the data input frame 130 contains values only in the single-value data entry column 126, the output is directed to the data output frame 150. And as previously discussed, if either the string-of-values data entry column 128, or the range-of-value data entry column 138 contains data, the output will be placed in a delimited text file (such as is suitable for importing into

spreadsheet or word processing programs) and the user receives the results following the completion of the calculations.

The data output frame 150d contains one column of data showing the percent difference between devices given as a one-sigma standard deviation number, although this is user definable. All process parameter contributions are given as one-sigma standard deviation numbers and these parameters are combined as a root-sum-of-squares to generate the total mismatch 162. As before, the (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution.

Capacitor Scenario

Referring to Fig. 9, an interface screen showing the data entry input frame and mismatch results output frame for a capacitor mismatch calculation scenario is shown. The interface screen 100, as previously discussed, comprises a calculation setup frame 110, a data input frame 130, a data output frame 150, and a message frame 158. In the capacitor calculation scenario in an embodiment of the present invention, the user will select a device type selection 114 designating a capacitor (abbreviated "CAP" in Fig. 9. Following completion of the selections of the desired technology and the create data entry

input form 120 button in the calculation setup frame 110, the data input frame 130 is generated.

The data entry input frame 130 comprises length and width selection parameters 132. The specific length and width parameters 132 that are generated following the selection of the create data entry input form 120 button are dependent upon the previous technology and device selections and therefore may vary. As previously discussed, the desired values for the width and length parameters may be entered into the single-value data entry column 126, the string-of-values data entry column 128, and the range-of-value data entry column 138 in any combination of the three columns. And as before, if multiple columns contain data entries for the same width and length parameters, the calculation precedence is established from right to left (i.e. the range-of-value data entry column 138 supercedes the string-of-values data entry column 128 which in turn supercedes the single-value data entry column 126.

Below the input columns for width and length, the user can choose to simulate the mismatch pair in a cross-couple configuration by entering appropriate data values into cross-coupled configuration data entry fields 134 that are comprised of fields for Center-to-center and Sigmas(#). It should be noted that the process for computing the mismatch is a little different for the capacitor scenario then that of the transistor

scenarios. The primary difference is that a SPICE or MCSPICE type program is not utilized as the calculation is much simpler. Instead, a parameter file is used for the measured data terms.

An additional difference is the equation for computing the mismatch. The computational code for this mismatch calculation is: $(\sigma_R^2/R^2) = (\sigma_L^2/L^2) + (\sigma_w^2/W^2) + (\sigma_{LW}^2/LW) + (g*ctc^2)$.

Following the calculation of the capacitor scenario, if the data input frame 130 contains values only in the single-value data entry column 126, the output is directed to the data output frame 150. And as previously discussed, if either the string-of-values data entry column 128, or the range-of-value data entry column 138 contains data, the output will be placed in a delimited text file (such as is suitable for importing into spreadsheet or word processing programs) and the user receives the results following the completion of the calculations.

The data output frame 150e contains one column of data showing the percent difference between devices given as a one-sigma standard deviation number, although this is user definable. All process parameter contributions are given as one-sigma standard deviation numbers and these parameters are combined as a root-sum-of-squares to generate the total mismatch 162. As before, the (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution.

While the invention has been particularly shown and described with reference to the embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made therein without departing from the spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A mismatch modeling tool comprising:

a software implemented transistor mismatch model;

at least one editable mismatch model data library comprising process parameter variables accessed by said software implemented transistor mismatch model;

a circuit simulation library and program data output accessed by said software implemented transistor mismatch model; and

a graphical interface to said software implemented transistor mismatch model.

2. The mismatch modeling tool of Claim 1 wherein said graphical interface comprises a menu driven modeled device selection frame.

3. The mismatch modeling tool of Claim 2 wherein said menu driven modeled device selection frame configures said software implemented transistor mismatch model to display a dynamically generated input data frame within said graphical interface.

4. The mismatch modeling tool of Claim 3 wherein said dynamically generated input data frame reflects data input fields of one of a plurality of input scenarios comprising at least one of:

a voltage driven scenario;

a current driven scenario;

a differential pair scenario;

a resistor scenario; and

a capacitor scenario.

5. The mismatch modeling tool of Claim 4 wherein said dynamically generated input data frame comprises a plurality of data input columns comprised of at least one of:

a plurality of single-data input parameter fields;

a plurality of string-of-data input parameter fields; and

a plurality of range-of-data input parameter fields.

6. The mismatch modeling tool of Claim 5 further comprising an electronically transmitted ASCII output data file, said ASCII output data file comprising output data reflecting at least one of:

said plurality of single-data input parameter fields;

said plurality of string-of-data input parameter fields; and

said plurality of range-of-data input parameter fields.

7. The mismatch modeling tool of Claim 6 wherein said ASCII output data file is an emailed ASCII output data file.

8. The mismatch modeling tool of Claim 6 further comprising a three dimensional output plot, said three dimensional output plot being a graphical representation of said output data within said ASCII output data file.

9. The mismatch modeling tool of Claim 5 further comprising a dynamically generated output data frame, said dynamically generated output data frame displaying output data reflecting said plurality of single-data input parameter fields.

10. A mismatch modeling tool comprising:

a software implemented transistor mismatch model;

at least one editable mismatch model data library comprising process parameter variables accessed by said software implemented transistor mismatch model; and

a circuit simulation library and program data output accessed by said software implemented transistor mismatch model.

11. The mismatch modeling tool of Claim 10 further comprising a graphical interface to said software implemented transistor mismatch model.

12. The mismatch modeling tool of Claim 11 wherein said software implemented transistor mismatch model is configurable for a plurality of input scenarios comprising at least one of:

a voltage driven scenario;

a current driven scenario;

a differential pair scenario;

a resistor scenario; and

a capacitor scenario.

13. The mismatch modeling tool of Claim 12 wherein said graphical interface comprises a dynamically generated input data frame, said dynamically generated input data frame displaying parameters reflecting a selected said input scenario.

14. The mismatch modeling tool of Claim 13 wherein said dynamically generated input data frame comprises a plurality of data input columns comprised of at least one of:

a plurality of single-data input parameter fields;

a plurality of string-of-data input parameter fields; and

a plurality of range-of-data input parameter fields.

15. The mismatch modeling tool of Claim 14 further comprising a dynamically generated output data frame, said dynamically generated output data frame displaying output data reflecting said plurality of single-data input parameter fields.

16. The mismatch modeling tool of Claim 14 further comprising an electronically transmitted ASCII output data file, said ASCII output data file comprising output data reflecting at least one of:

said plurality of single-data input parameter fields;

said plurality of string-of-data input parameter fields; and

said plurality of range-of-data input parameter fields.

17. The mismatch modeling tool of Claim 16 further comprising a three dimensional output plot, said three dimensional output plot being a graphical representation of said output data within said ASCII output data file.

18. The mismatch modeling tool of Claim 13 wherein said dynamically generated input data frame comprises a plurality of data input columns comprised of at least one of:

a plurality of string-of-data input parameter fields; and

a plurality of range-of-data input parameter fields.

19. The mismatch modeling tool of Claim 18 further comprising an ASCII output data file, said ASCII output data file comprising output data reflecting at least one of:

said plurality of string-of-data input parameter fields; and

said plurality of range-of-data input parameter fields.

20. The mismatch modeling tool of Claim 19 further comprising a three dimensional output plot, said three dimensional output plot being a graphical representation of said output data within said ASCII output data file.

MISMATCH MODELING TOOL

ABSTRACT

A mismatch modeling tool (10) comprises a software implemented mismatch model (32). The software implemented mismatch model (32) accesses: at least one editable mismatch model data library (18) comprising process parameter variables, and circuit simulation library and program (14) data output. An interface screen (100) provides input and output coupling between a user and the software implemented mismatch model (32).

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.